AMENDMENTS TO THE CLAIMS

Please amend claims 2-3 and add new claims 9-20 as shown in the following list of claims.

1. (Original) A semiconductor memory device comprising:

a redundant memory cell for use instead of a memory cell when the memory cell has a defect;

an electrode applied with a test signal for setting a test condition from outside in testing the redundant memory cell; and

an output circuit for outputting data read out of the memory cell and the redundant memory cell,

wherein when the test signal is applied to the electrode to set the test condition for the redundant memory cell, the output circuit is configured to output data read out of the redundant memory cell at a level different from a signal level of data read out of the memory cell for output.

2. (Currently Amended) The [[A]] semiconductor memory device according to claim 1, wherein when the test condition for the redundant memory cell is set, the output circuit outputs the data read out of the redundant memory cell of high-level potential at a lower potential than a predetermined voltage.

3. (Currently Amended) The [[A]] semiconductor memory device according to claim 1, wherein when the test condition for the redundant memory cell is set, the output circuit inverts and outputs data read out of the redundant memory cell.

4. (Original) The semiconductor memory device according to claim 1, wherein the output circuit comprises:

a first logic gate for determining that both the test signal and an internal control signal created based on the test signal have normal logical values; and

a second logic gate for inverting and outputting the data read out of the redundant memory cell based on an output signal of the first logic gate.

5. (Original) A semiconductor memory device comprising:

first and second redundant memory cells for use instead of a memory cell when the memory cell has a defect;

first and second electrodes applied with a test signal for setting a test condition from outside in testing the first and second redundant memory cells; and

an output circuit for outputting data read out of the memory cell and the first and second redundant memory cells,

wherein when the test signal is applied to both the first and second electrodes to set the test condition for the first and second redundant memory cells, the output circuit is configured to output a signal at a fixed level.

6. (Original) The semiconductor memory device according to claim 5, wherein when the test condition for the first and second redundant memory cells is set, the output circuit outputs a signal at high level or low level.

7. (Original) The semiconductor memory device according to claim 5, wherein the output circuit comprises:

a first logic gate for determining that the test signal for the first and second redundant memory cells and an internal control signal created based on the test signal have all normal logical values; and

a second logic gate for fixing an output signal at high level or low level by an output signal of the first logic gate when a normal test condition is set.

8. (Original) A semiconductor memory device comprising:

a redundant memory cell for use instead of a memory cell when the memory cell has a defect;

an electrode applied with a test signal for setting a test condition from outside in testing the redundant memory cell; and

an output circuit for outputting data read out of the memory cell and the redundant memory cell,

wherein when the test signal is applied to the electrode to set the test condition for the redundant memory cell, the output circuit is configured to output data read out of the redundant memory cell at timing different from timing to output data read out of the memory cell.

9. (New) The semiconductor memory device according to claim 1, wherein the output circuit includes:

a first gate circuit having an input terminal for receiving the test signal and an output terminal for outputting an internal control signal;

a second gate circuit having a first input terminal for receiving the internal control signal and a second input terminal for receiving the data read out of the memory cell and the redundant memory cell and an output terminal; and

an inverter having an input terminal connected to the output terminal of the second gate circuit and an output terminal.

10. (New) The semiconductor memory device according to claim 9, wherein the first gate circuit is an AND circuit.

11. (New) The semiconductor memory device according to claim 9, wherein the second gate circuit is an exclusive NOR circuit.

12. (New) The semiconductor memory device according to claim 1, wherein the output circuit includes:

an inverter having a first power terminal connected to receive a first power potential, a second power terminal connected to receive a second power potential, an input terminal for receiving the data read out of the memory cell and the redundant memory cell and an output terminal;

a gate circuit having an input terminal for receiving the test signal and an output terminal for outputting an internal control signal; and

a control circuit connected to the first power terminal of the inverter, the control circuit reducing a voltage of the first power potential in accordance with the internal control signal.

13. (New) The semiconductor memory device according to claim 12, where in the gate circuit is a NAND circuit.

14. (New) The semiconductor memory device according to claim 12, wherein the control circuit has a PMOS transistor connected between the first power terminal of the inverter and the first power potential, and wherein the control PMOS transistor has a gate connected to the output terminal of the gate circuit.

15. (New) The semiconductor memory device according to claim 5, wherein the output circuit includes:

a first gate circuit having an input terminal for receiving the test signal and an output terminal for outputting an internal control signal;

a second gate circuit having a first input terminal for receiving the internal control signal and a second input terminal for receiving the data read out of the memory cell and the redundant memory cell and an output terminal; and

an inverter having an input terminal connected to the output terminal of the second gate circuit and an output terminal.

16. (New) The semiconductor memory device according to claim 15, wherein the first gate circuit is a NAND circuit.

17. (New) The semiconductor memory device according to claim 15, wherein the first gate circuit is an AND circuit.

18. (New) The semiconductor memory device according to claim 15, wherein the second gate circuit is a NAND circuit.

19. (New) The semiconductor memory device according to claim 15, wherein the second gate circuit is a NOR circuit.

20. (New) The semiconductor memory device according to claim 8, wherein the output circuit includes an output timing control circuit for controlling a timing for outputting the data read out of the redundant memory cell.